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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/196,136	11/20/98	OHBAYASHI S	49657-217

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ART UNIT	**PAPER NUMBER**
2133	2

DATE MAILED: 01/19/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

PTO-90C (Rev. 2/95)
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1- File Copy

Office Action Summary	Application No. 09/196,136	Applicant(s) OHBAYASHI	
	Examiner Guy J Lamarre, P.E.	Art Unit 2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 November 1998* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *1* .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other:

DETAILED ACTION

1. Claims 1- 18 are presented for examination.

Claim Rejections - 35 USC ' 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2.1 **Claims 1-10** are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants' Admitted prior art **(hereinafter** Admitted prior art) in view of **Ruparel et al.** (A vertically integrated test methodology based on JTAG IEEE 1149.1 Standard Interface; **IEEE,** 27 Sept. 1991).

As per Claim 1, Admitted prior art substantially discloses the claimed semiconductor integrated circuit (fig. 17) comprising: a boundary scan test circuit (165) for testing, after said semiconductor integrated circuit is mounted on a printed circuit board, the mounted state; a first pad (TMS) having a potential level set according to a type of a package in which said semiconductor integrated circuit is sealed; and control circuitry (165) for fixedly setting said boundary scan test circuit to either one of an operable state and an operation disabled state according to the potential level of said first pad.{See **Admitted prior art,** Figs.11A-20, and page 1 line 12 – page 16 line 3, in passim, wherein semiconductor integrated circuit and method are described.} **Not specifically described** in detail in **Admitted prior art** is the step of a boundary scan test circuit (165) for testing, after said semiconductor integrated circuit is mounted on a printed circuit board, the mounted state. However **Ruparel et al.,** in an analogous art, discloses a test methodology based on JTAG IEEE 1149.1 Standard Interface wherein such techniques are described {See **Ruparel et al.,** Id., Abstract lines 3- end} **Therefore,** it would have been obvious to a person having ordinary skill in the art at the time the invention was made

to modify the procedure in the **Admitted prior art** by including therein a test methodology as taught by **Ruparel et al.,** because such modification would provide the procedure disclosed in **Admitted prior art** with a technique wherein "*the test methodology accomplishes testing at all levels ranging from the wafer level up to the board and system levels.*" {See **Ruparel et al.,** Conclusion: last paragraph.}

As per Claim 2, Ruparel et al. teaches the procedure for the claimed semiconductor integrated circuit according to claim 1, wherein said boundary scan test circuit comprises a buffer circuit coupled to a second pad to generate an internal signal according to an externally applied signal via said second pad in an operable state, and said control circuitry comprises a circuit for selectively setting said buffer circuit to the operable state or to the operation disabled state in accordance with the potential level at said first pad.{See **Ruparel et al.,** Id., Fig. 1 and related description on page 11-4.2, col. 1, para. 2, lines 3-end, wherein storage means is described to effect testing.}

As per Claim 3, Admitted prior art teaches the procedure for the claimed semiconductor integrated circuit according to claim 1, wherein said type of the package includes a surface mount type flat package and a solder ball array arrangement type package {See **Admitted prior art,** Id., page 2 lines 19-end for package type selection means. Also refer to **Ruparel et al.,** Id., page 11-4.2, col. 2, para. 3, lines 1-end.}

As per Claim 4, Admitted prior art teaches the procedure for the claimed semiconductor integrated circuit according to claim 3, wherein said control circuitry includes a circuit for setting said boundary scan test circuit to the operable state when the type of the package is the solder ball array arrangement type package and to the operation disabled state when the type of the package is the surface mount type flat package {See **Admitted prior art,**

Id., Fig. 16 and page 8 lines 7-end for boundary scan test circuit setting means. Also refer to **Ruparel et al.,** Id., page 11-4.3, col. 1, para. 3, lines 1-end.}

As per Claim 5, Ruparel et al. teaches the procedure for the claimed semiconductor integrated circuit according to claim 2, wherein the type of the package includes a surface mount type flat package and a solder ball array arrangement type package, and said control circuitry includes a circuit for setting said buffer circuit into the operable state when the type of the package is the solder ball array arrangement type package and to the operation disabled state to fix an output signal of said buffer circuit to a predetermined logical level when the package is the surface mount type flat package {See **Ruparel et al.,** Id., page 11-4.2, col. 2, para. 4, lines 1-end, wherein means is provided for package selection, and for setting buffer circuitry or data storage.}

As per Claim 6, Ruparel et al. teaches the procedure for the claimed semiconductor integrated circuit according to claim 1, wherein said boundary scan test circuit comprises a first logic gate having a first input coupled to a second pad and a second input, said control circuitry comprises a first set circuit for generating a signal of a potential according to a potential of said first pad, and a second logic gate applying a signal to the second input of said first logic gate that sets said first logic gate to one of the operable state and the operation disabled state, according to an output signal of said first set circuit.{See **Ruparel et al.,** Id., page 11-4.3, col. 1, last para., lines 1-end, wherein means is provided for scan operation control.}

As per Claim 7, Ruparel et al. teaches the procedure for the claimed semiconductor integrated circuit according to claim 6, wherein said first set circuit includes means for generating a function setting signal for setting a function implemented by said semiconductor integrated circuit in accordance with the potential at said first pad {See **Ruparel et al.,** Id., page 11-4.3, col. 1, last para., lines 1-end, wherein means is provided for scan operation control.}

As per Claim 8, Ruparel et al. teaches the procedure for the claimed semiconductor integrated circuit according to claim 6, wherein said first set circuit includes means for generating an operation mode designation signal placing the semiconductor integrated circuit in an operation mode designated by said operation mode designated signal {See **Ruparel et al.,** Id., page 11-4.2, col. 1, 2^{d} para., lines 1-end, wherein means is provided for testing control.}

As per Claim 9, Ruparel et al. teaches the procedure for the claimed semiconductor integrated circuit according to claim 1, wherein said boundary scan test circuit comprises a first logic having a first input coupled to a second pad and a second input, said control circuitry comprises a first set circuit for generating a signal of a potential according to a potential of said first pad, a second set circuit for generating a signal of a potential according to a potential of a third pad, and a second logic gate receiving an output signal of said first set circuit and an output signal of said second set circuit to perform a logic process thereon, and applying a resultant signal to the second input of said first logic gate.{See **Ruparel et al.,** Id page 11-4.2, col. 2, Package testing.}

As per Claim 10, Ruparel et al. teaches the procedure for the claimed semiconductor integrated circuit according to claim 6, wherein said function set circuit comprises a first transistor for setting said first pad to a first logic level in response to starting of application of power supply voltage, an inverter circuit inverting a logic level of the potential of said first pad to output a signal corresponding to an output signal of said first set circuit, and a second transistor connected in parallel to said first transistor, between said first pad and a power source node applying a potential of said first logic level, and receiving an output signal of said inverter circuit at a control electrode node thereof {See **Ruparel et al.,** Id., page 11-4.2, col. 1, 2^{d} para., lines 1-end, wherein means is provided for testing control.}

2.2 **Claim 11** is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants' Admitted prior art **(hereinafter** Admitted prior art) in view of **Ruparel et al.** (A vertically integrated test methodology based on JTAG IEEE 1149.1 Standard Interface; **IEEE,** 27 Sept. 1991) in further view of **Iketani et al**. (US Patent No. 5,703,510, Feb. 1996).

As per Claim 11, Admitted prior art and **Ruparel** substantially disclose the claimed semiconductor integrated circuit according to claim 9, wherein said second set circuit comprises a first transistor for setting said third pad to the potential level of a first logic level in response to starting of application of a power supply voltage, an inverter circuit inverting a logic level of a potential of said third pad to output a signal corresponding to an output signal of said second set circuit, and a second transistor connected in parallel to said first transistor, between said third pad and a power source node applying a potential at said first logic level, and receiving an output signal of said inverter circuit (Prior Art Fig. 19) at a control electrode node thereof. {See **Ruparel et al.,** Id page 11-4.2, col. 2, Package testing, and **Admitted prior art,** Figs.11A-20, and page 1 line 12 – page 16 line 3, in passim, wherein semiconductor integrated circuit and method are described.} **Not specifically described** in detail, in the **Admitted prior art** and **Ruparel et al.,** is an inverter circuitry means for inverting logic levels of voltages. However **Iketani et al.,** in an analogous art, discloses such techniques. {See **Iketani et al.,** Id., Abstract and Fig. 2.} **Therefore**, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the procedure in the **Admitted prior art** and **Ruparel et al.,** by including therein inverter circuitry means as taught by **Iketani et al.,** because such modification would provide the procedure disclosed in the **Admitted prior art** and **Ruparel et al.,** with a technique whereby "*erroneous activation of power can be prevented.*" {See **Iketani et al.,** col. 3, lines 55-56.}

2.3 **As per Claims 12-18,** the limitations are similar to the ones of **Claims 1-11** except for absence of scanning means. **Claims 12-18** are rejected under 35 U.S.C. 103(a) as being

unpatentable over Applicants' Admitted prior art **(hereinafter** Admitted prior art) in view of **Ruparel et al.** (A vertically integrated test methodology based on JTAG IEEE 1149.1 Standard Interface; **IEEE,** 27 Sept. 1991) in further view of **Iketani et al**. (US Patent No. 5,703,510, Feb. 1996), based on the same rationale as the rejection of **Claim11.**

2.4 Examiner requests that Applicant provide information on any copending applications that may raise **double patenting** issues with instant application. Examiner requests that Applicant provide information **English translation of IDS reference by Nikkei Electronics** for review in response to present Office Action.

Specification

3. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors, e.g., "when operates" on line 11 page 19. Applicant's cooperation is requested in correcting any errors which applicant may become aware of in the specification.

3.1 The disclosure is objected to because line 7 page 19 of the specification refers to circuit **30**, not shown in Fig. 1. Said circuit should apparently be **3**. Appropriate correction is required.

Claim Objections

4. The claim 14 line 3 is objected to for "paid." Said term should apparently be "**pad**." Appropriate correction is required.

Claim Rejections - 35 USC § 112 SECOND PARAGRAPH

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5.0. **Claims 1** and **12,** and all intervening claims, are rejected under 35 U.S.C. § 112 SECOND PARAGRAPH for being indefinite.

5.1. There is insufficient antecedent basis for the limitation "protector" in Claim 15 line 3 and intervening claims: input signal had not been previously defined.

5.1.1 It is unclear what the limitation "thereof" refers to in Claim 15 line 4.

5.2. It is unclear what the limitation "thereof" refers to in Claim 13 line 4.

5.3. It is unclear **to** what component the power supply is connected to in Claim 12 line 4. Is it connected to the pad or to the first transistor?

5.3.1 It is unclear what operation mode of internal circuit is in Claim 12 lines 9-10.

5.3.2 It is unclear how inverter is operatively connected to the pad in Claim 12 line 5.

5.4 It is unclear what mounted state is in Claim 1 line 3.

5.4.1 It is unclear what limitation means in Claim 1 lines 7-8, e.g., first pad with potential level according to a type of package.

5.4.2 It is unclear how the rest of the semiconductor is operatively connected to the first pad in Claim 1.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The references are cited in Form PTO-892 for the Applicant's review.

6.1 Any response to this action should be mailed to:

Commissioner of Patents and Trademarks, Washington, D.C. 20231

or faxed to:

(703) 308-9051, (for formal communications intended for entry)

Or:

(703) 305-9724 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Guy Lamarre whose telephone number is (703) 305-0755. The examiner can normally be reached on Monday to Friday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady, can be reached on (703) 305-9595.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Guy Lamarre, P.E.

Patent Examiner

01/16/01

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